Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously amended) A message memory equipped with:

- a logical, virtual memory representation for a configurable number of message-object memories and their data capacity for the storage of message contents,

- a physical memory divided into a specific number of segments,

characterized in that the data capacity of the individual message-object memories and their association with the segments of the physical memory are configurable,

wherein a physical access address of the physical memory comprises least significant bits from a logical address of a message-object memory and least significant bits from a logical byte address within the message-object memory.

2. (original) A message memory as claimed in claim 1, characterized in that a message object takes the form of a cluster of multiple memory segments.

3. (previously presented) A message memory as claimed in claim 1, characterized in that predetermined configurations are defined in the application software.

4. (previously amended) A method of defining the association between the logical representation and the physical memory for a message memory equipped with:

- a logical, virtual memory representation for message-object memories with a plurality of data fields for the storage of message contents,

- a physical memory divided into a specific number of segments,

characterized by the following steps:

- determination of the length of a message content in bytes,

- selection of a number of memory segments per cluster as a function of the byte length of the message content, wherein a cluster forms a message-object memory,

wherein a physical access address of the physical memory comprises least significant bits from a logical address of a message-object memory and least significant bits from a logical byte address within the message-object memory.

5. (cancelled).

6. (previously added) A message memory as claimed in claim 1, wherein the physical access address of the physical memory comprises the five least significant bits from the logical address of the message-object memory and the three least significant bits from the logical byte address within the message-object memory.

7. (previously added) A message memory as claimed in claim 1, wherein the physical access address of the physical memory comprises the three least significant bits from the logical address of the message-object memory and the five least significant bits from the logical byte address within the message-object memory.

8. (previously added) A message memory as claimed in claim 1, wherein the physical access address of the physical memory comprises the two least significant bits from the logical address of the message-object memory and the six least significant bits from the logical byte address within the message-object memory.

9. (previously added) The method of claim 4, wherein the physical access address of the physical memory comprises the five least significant bits from the logical address of the message-object memory and the three least significant bits from the logical byte address within the message-object memory.

10. (previously added) The method of claim 4, wherein the physical access address of the physical memory comprises the three least significant bits from the logical address of the message-object memory and the five least significant bits from the logical byte address within the message-object memory.

11. (previously added) The method of claim 4, wherein the physical access address of the physical memory comprises the two least significant bits from the logical address of the message-object memory and the six least significant bits from the logical byte address within the message-object memory.

12. (previously added) A message memory equipped with:

- a logical, virtual memory representation for a configurable number of message-object memories and their data capacity for the storage of message contents,

- a physical memory divided into a specific number of segments,

characterized in that the data capacity of the individual message-object memories and their association with the segments of the physical memory are configurable,

wherein the number of address bits of a logical address of a message-object memory and the number of address bits of a logical byte address within the message-object memory are determined by the maximum upper limit of an address space of the message memory.

13. (previously added) A message memory as claimed in claim 12, wherein an access of a protocol controller or of a central processing unit interface to the message memory takes place via the logical, virtual memory representation independently of the configuration of a) logical addresses of the configurable number of message-object memories and b) logical byte addresses within the configurable number of message-object memories.